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# **VTAP25 Integration Guide**

Firmware from v2.3.0.2

VTAP25-MOD

Revised June 2025 v0.91



**If you need help** to set up or use your VTAP25 module, beyond what is contained in this Integration Guide, then please contact our support team.

Email: <a href="mailto:vtap-support@dotorigin.com">vtap-support@dotorigin.com</a>

Download the latest documentation and firmware from https://vtapnfc.com

Telephone UK and Europe: +44 (0) 1428 685861

Telephone North America and Latin America: +1 (562) 262-9642

**If you have any feedback** on setting up or using your VTAP25 module or this documentation, then please contact our support team. The product is constantly being reviewed and improved and we value feedback about your experience.

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Dot Origin Ltd Unit 7, Coopers Place Business Park, Combe Lane, Wormley Godalming GU8 5SZ United Kingdom +44 (0) 1428 685861

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# **Safety instructions**

#### WARNING: INTENDED USE

The VTAP25 module is intended for use by suitably qualified integrators, who will integrate the VTAP25-MOD (surface mount module) into their own hardware, without any changes or modifications to the VTAP25-MOD device. The module is not user-serviceable.

#### WARNING: ESD PRECAUTIONS

We recommend careful handling and storage of Electrostatic Sensitive Devices (ESDs) during installation. The VTAP25-MOD surface mount module should always be protected by static shielding bags for shipping or storage.

#### WARNING: POWER SUPPLY

Follow the power supply options described in Section 5.1 Power

EMC emissions and immunity certifications are only valid when using the VTAP25-MOD reader module in accordance with these instructions.

#### WARNING: FCC COMPLIANCE

Certification in progress - conditions will apply to preserve compliance after integration.

## 1 Using this guide

This guide contains the information you need to integrate the VTAP25-MOD reader module into your host hardware.



Figure 1-1 VTAP25-MOD reader module

Consult the other VTAP Guides and Application Notes for more information about configuration methods and communication protocols, including how to update the firmware on your VTAP25 unit, when a new release is available.

If you need help with VTAP25-MOD reader module integration beyond what is contained in this guide please contact **vtap-support@dotorigin.com**.

## 1.1 Key features

- Power supply: 3.3V or 5V DC with on-board power management and USB VBUS detection
- Dimensions: 24mm x 29.3mm x 5.9mm (0.95in x 1.15in x 0.23in)
- Castellated (half-holes) SMD mounting (1.5mm pitch)
- Frequency/standards: 13.56MHz, ISO 14443A/B, ISO 15693 and ISO 18092
- Read capabilities: Apple Wallet (VAS and ECP2), Google Wallet (Smart Tap and HCE), NFC Type 1-5, MIFARE® Classic, MIFARE Ultralight, MIFARE DESFire, NTAG.
- Other NFC modes: Dynamic NFC tag emulation; GymKit handoff
- Operator feedback:

- Buzzer output signal (3.3V logic)
- Serial LED output signal (3.3V logic)
- Connectivity:
  - USB interface (mass storage, Human Interface Device, USB Virtual COM port)
  - Serial interfaces including UART, SPI slave, I<sup>2</sup>C slave all 3.3V
  - UART supports external TTL, RS-232 and/or RS-485 level converters
  - All serial interfaces support both VTAP protocol (passive or active) and OSDP (standard and secure)
- Security: Programmable secure element (reserved for future use)

Please refer to the VTAP25 datasheet and other VTAP documentation for additional information.

# 2 Block diagram

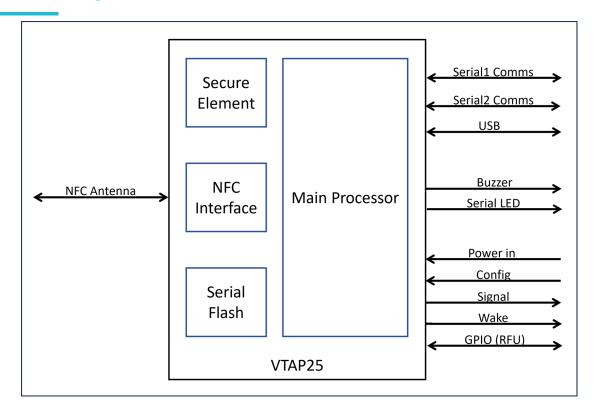
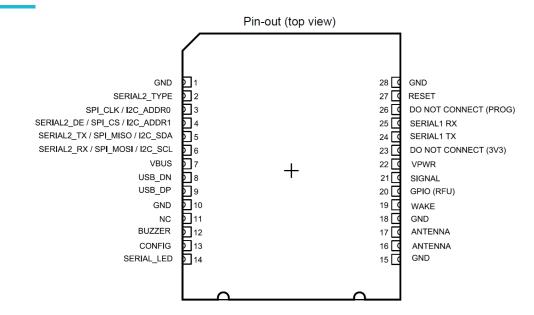


Figure 2-1 VTAP25 Block diagram

# 3 Pin description



#### Figure 3-1 VTAP25 Pin out (Top left corner bevelled to indicate pin 1)

Pin no.	Pin name	Туре	Description
1	GND	Power supply	
2	SERIAL2_TYPE	Input	Input I2C or SPI selection. Pull low for SPI, high for I2C
3	SPI_CLK / I2C_ ADDR0	Input	Configurable: SPI clock input Determines LSB of I2C address - tie to GND to clear LSB, tie to 3V3 to set LSB
4	SERIAL2_DE / SPI_ CS / I2C_ADDR1	Input	Configurable: Serial comms data enable to drive EIA485 transceiver SPI chip select. Pull low to select. Determines LSB-1 of I2C address - tie to GND to clear LSB-1, tie to 3V3 to set LSB-1
5	SERIAL2_TX / SPI_ MISO / I2C_SDA	Input/Output	Configurable: Serial comms transmit (3V3 logic) I2C data input / output. (Pull up resistors must be fitted on host board) SPI data output
6	SERIAL2_RX / SPI_ MOSI / I2C_SCL	Input/Output	Configurable: Serial comms receive (3V3 logic) I2C clock input. (Pull up resistors must be fitted on host board) SPI data input
7	VBUS	Power	USB 5V - note this does not power the module, only for data enable
8	USB_DN	Input/Output	USB data
9	USB_DP	Input/Output	USB data
10	GND	Power supply	
11	NC	-	

Pin no.	Pin name	Туре	Description	
12	BUZZER	Output	3V3 logic drive for external buzzer - variable frequency, 50/50 mark/space	
13	CONFIG	Input	Pull low to bypass config.txt on startup	
14	SERIAL_LED	Output	Serial LED 3V3 logic output - 'Neopixel' protocol. Host must provide 5V driver	
15	GND	Power supply		
16	ANTENNA	Input/Output	Connect to antenna via matching circuit	
17	ANTENNA	Input/Output	Connect to antenna via matching circuit	
18	GND	Power supply		
19	WAKE	Output	Driven high when a payload is available to be read and can be used to wake up the host processor	
20	GPIO (RFU)	Input/Output	Reserved for future use. Recommended to connect this pin to host GPIO so the functionality could be used when released.	
21	SIGNAL	Output	Flag signal for data availability on the host connected serial interface (I2C/SPI)	
22	VPWR	Power supply	Power to module. 3.3V to 5V	
23	DO NOT CONNECT (3V3)	-		
24	SERIAL1_TX	Output	Serial comms transmit	
25	SERIAL1_RX	Input	Serial comms receive	
26	DO NOT CONNECT (PROG)	-		
27	RESET	Input	Pull low to reset module	
28	GND	Power supply		

The VTAP25-MOD reader module has no antenna. Before you can use any VTAP reader functionality, it requires connection of an external antenna, with a suitable matching circuit.

# 4 Environmental specification

### 4.1 Storage

Ambient temperature: -40 to +125°C (-40 to 257°F) Humidity: 0 to 95% RH non-condensing Pressure: 86-106kPa

## 4.2 Maximum ratings

Power supply: 5.5V DC VBUS: 5.5V DC All I/O: 3.5V DC Antenna current: TBC

## 4.3 Recommended operating conditions

Power supply: 3.3V or 5V DC Ambient temperature: -40 to +85°C (-40 to 185°F) Humidity: 0 to 95% RH non-condensing Pressure: 86-106kPa

# 4.4 Operating specifications

Supply current: TBC Wake-up time: 1 sec (configurable)

# 5 Electrical integration

#### 5.1 Power

The following power connection scenarios are available:

#### Powered from Host PSU, no USB connectivity

The module is powered from host PSU on VPWR pin. Input voltage can be 3.3V to 5V.

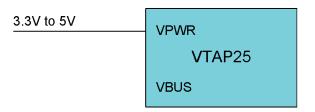


Figure 5-1 VTAP25 powered from host PSU

#### Powered from USB

The module is powered from USB on VPWR pin. VBUS is connected to the USB 5V.

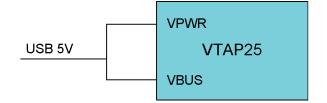
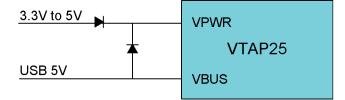


Figure 5-2 VTAP25 powered from USB

#### Powered from Host, but USB may be plugged in and can power the module

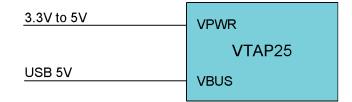
In this scenario, the module is powered from host PSU, but USB may be plugged in at some point and can power the module.





#### Powered from Host, but USB may be plugged in but NOT power the module

In this scenario, the module is powered from host PSU. USB may be plugged in at some point but will NOT power the module.



#### Figure 5-4 VTAP25 powered from host PSU with USB that does not supply power

#### 5.2 NFC antenna

As the VTAP25 does not have an NFC antenna, an external matched NFC antenna must be connected to the VTAP25 module to use any VTAP functionality. The antenna can be an off-the-shelf or a custom antenna depending on the project requirements and level of RF design expertise available.

Your choice of NFC antenna will be affected by the type of enclosure you are designing to house the VTAP25 module and the NFC antenna, the desired user experience, and your approach to radio testing and certification of your end product.

- a. Integrate a suitable tuning circuit into your own antenna assembly;
- b. Design a separate tuning circuit that can be mounted in between the VTAP25 module and off-the-shelf external antenna

Also pay special attention to the type of the NFC antenna, if it is to be mounted very close to a metal surface / LCD screen.

**CAUTION:** Always ensure sufficient clearance between the NFC antenna and other RF transmitters, to avoid electromagnetic interference between equipment. Clearance required varies between antennas, depending on antenna size, power and sensitivity.

If you have not yet chosen or designed an antenna and matching circuit, Dot Origin can provide support for integrating off-the-shelf or custom NFC antennas with the VTAP25 in your device, contact **vtap-support@dotorigin.com**.

#### 5.2.1 Antenna matching

A matching or tuning circuit ensures that there is optimum power transmitted between the module and the antenna, Tuning is essential to NFC transmission, since imperfect antenna matching or tuning can cause high power loss and poor antenna performance.

Multiple factors can affect the antenna matching, including length of the conductor between the VTAP25 module, matching circuit and the antenna, the size of the antenna and any nearby metal objects. Hence the antenna tuning process should be carried out with the antenna fitted into the final product and mounted in a manner representative of normal use.

Important considerations and examples of tuning circuits suited to specific off-the-shelf antennas are provided in the VTAP Application Note about external antennas.

The VTAP25 has test pads on the bottom of the module for connecting a Vector Network Analyser (VNA) to measure antenna tuning parameters.

See the Reference schematics section for an example NFC antenna circuit. The values of resistors and capacitors are determined during the antenna matching.

These are the main steps involved in antenna matching circuit design and verification:

- Find the antenna characteristics of your antenna. This is done by finding DC resistance, self-resonance frequency and inductance of the antenna. These measurements are carried out with the antenna disconnected from the matching circuit. This may involve removing matching circuit components.
- 2. Calculate the series and parallel capacitor values.
- Test circuit performance by measuring S11 impedance into the antenna circuits (includes filters, matching circuit and antenna). Use the test pads on the bottom of the module to access these nodes.

Although the VTAP25 uses a later generation of NFC front end chip, it is useful to refer to NXP's Application Note #AN13219 **PN7160 antenna design and matching guide** for calculations and further help.

#### 5.2.2 Antenna connection

If the antenna is part of the PCB copper, tracks from the VTAP25 to the antenna should not exceed 100mm per track. The tracks should be routed as close together as possible to minimise loop area.

The antenna matching circuit may be placed near the VTAP25 or near the antenna. It should not be placed at a midpoint.

It is recommended that any circuits are at least 5mm from antenna tracks. If circuits are placed within the antenna area, a ground plane should be used in the component area, but should be kept as far from the antenna wiring as possible. Circuit connections may cross antenna tracks, but should crossings should be perpendicular.

**CAUTION:** Placing connected circuits inside and outside the antenna area, such that tracks cross the antenna, is likely to increase unwanted radiated emissions.

Where the antenna is to be connected by wires, it is recommended that tracking between the VTAP25 and connection point of wiring should be as short as possible and not exceed 40mm. Wiring should be twisted pair. It is recommended that you avoid bundling antenna connections with other product wiring. Connectors for wiring do not need to be specialised - simple pin header parts will usually suffice. It is recommended that you avoid connectors where the conductors are more than 3mm apart.

#### 5.3 Hardware reset

The VTAP25 does not require an external reset signal. However, it is recommended that pin 27 RESET is connected to a suitable GPIO on the host processor to allow it to force a reset of the VTAP25, should this be necessary. Connect pin 27RESET to the host and pull low to reset the VTAP25.

## 6 Peripherals

#### **6.1 Serial interfaces**

The VTAP25 reader module offers synchronous and asynchronous communications over two serial comm ports.

#### 6.1.1 SERIAL1

SERIAL1 allows asynchronous comms at 3V3 logic levels.

#### 6.1.2 SERIAL2

SERIAL2 may be configured for asynchronous comms, SPI or  $I^2C$  – all at 3V3 logic levels. By default, SERIAL2 will use synchronous communication (SPI or  $I^2C$ ) unless set asynchronous (UART) communications are configured explicitly in config.txt.

Use the module pin SERIAL2\_TYPE (Pin 2) to choose between SPI and I<sup>2</sup>C. Pull low for SPI, and pull high for I<sup>2</sup>C. The host board should connect the SERIAL2\_TYPE pin appropriately to select the required communication interface.

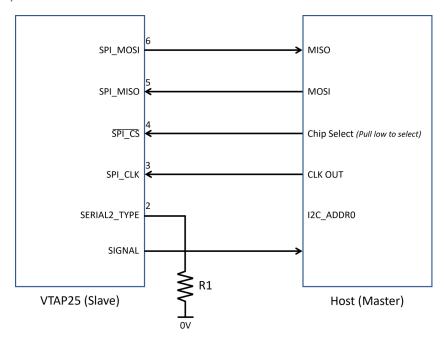


Figure 6-1 VTAP25 Serial2 SPI connection diagram

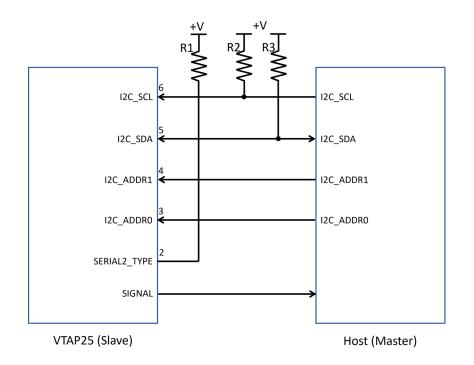


Figure 6-2 VTAP25 Serial2 I<sup>2</sup>C connection diagram

Asynchronous comms (3V UART) are enabled using the config.txt.

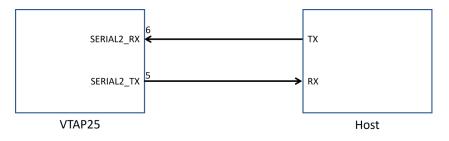


Figure 6-3 VTAP25 Serial2 UART connection diagram

Optionally, an RS-485 transceiver can be connected to SERIAL2\_TX, SERIAL2\_RX and SERIAL2\_DE (for transmit enable).

See the other VTAP guides and application notes for more information about configuration methods, communication protocols, settings and commands.

**Note:** It is recommended that you have a USB data connection (just 4 pins or test pads) provided on the host board to allow for firmware or config update/initialisation, in case communication with the host is not available via the preferred interface. For temporary use only, this can be just a direct connection to VBUS, D+, D- and GND (without USB inductors or suppression) for example via an unpopulated 4 way PCB header.

#### 6.2 USB

The USB interface is USB2.0. The VTAP25 appears as a removable drive, virtual ComPort (VCP) and Human Interface Device (HID) on USB. The config.txt file referred to elsewhere is stored on the removable drive. The VCP and HID modes can be configured using the config file.

USB interface is implemented even if it is not required for user function. This will allow access to the module for easy configuration / firmware upgrade if the preferred interface is not available.

If USB mass storage drive is required, ensure the LOCK pin is not pulled low as this will disable the mass storage.

#### 6.2.1 Recommendations for USB

USB layout rules should be followed. A filter and protection circuit is recommended - see NFC USB reader example for a reference circuit.

If connection is via USB-C, fit 5K1 resistor A5 to 0V and 5K1 resistor from B5 to 0V so that the host device can detect connectivity and power identification.

## 6.3 Serial LEDs

The device has serial LED output (Neopixel) for connecting a chain of up to 255 external serial LEDs. These can be configured to show a default colour permanently, and then automatically change colour (or flash) in response to a successful pass read, successful card read or error conditions. Custom LED sequences are also possible in response to successful reads.

The output is 3V3 logic and the host must provide 5V translation, as required. **The VTAP25 does not provide power for the LEDs.** See the example schematics for an external LED circuit diagram.

Refer to the other VTAP guides and application notes for more information on how to configure the serial LED output.

## 6.4 Buzzer

There is also a buzzer output for an external AC buzzer, which can be configured to beep on start-up, or in response to a successful pass or card read. The output is 3V3 logic drive (50/50 square wave) – user must provide the buzzer driver circuit. See the example schematics for an external buzzer circuit diagram.

Refer to other VTAP guides and application notes on how to configure the buzzer output.

## 6.5 Config bypass on startup

In a scenario where config.txt needs to be bypassed on startup, for example if SERIAL2 interface is erroneously changed to UART, where the physically connected interface is SPI

or I<sup>2</sup>C, you can pull the CONFIG pin (13) low to bypass the configuration on startup. This way the physically connected interface can be connected to the VTAP25 and config.txt can be updated.

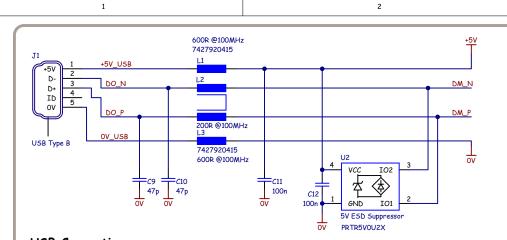
## 6.6 Signal

The signal output is used as a flag signal for when data is available to be transmitted on the Serial 2 interface (SPI or I<sup>2</sup>C). This allows the host to avoid continuous polling for data.

# 7 Reference schematics

## 7.1 VTAP25 USB example

This example schematic illustrates how to build a simple USB 2.0 reader using the VTAP25. It includes a buzzer circuit, serial LED level shifter and antenna with matching circuit.



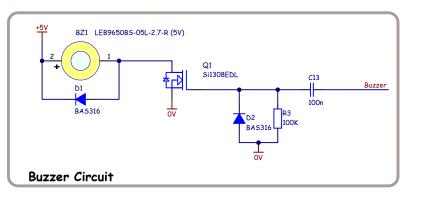
#### **USB** Connection

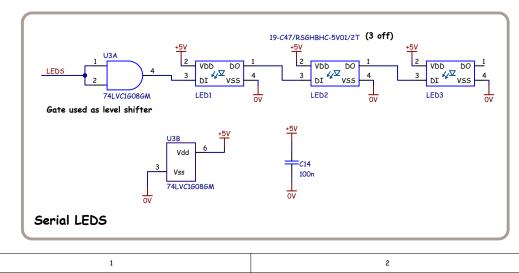
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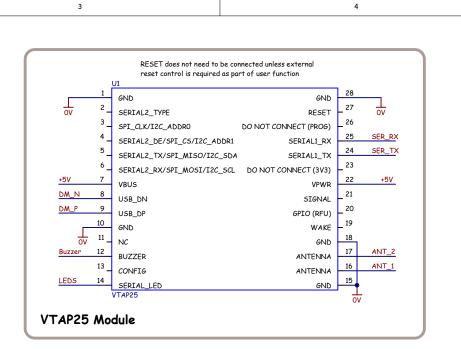
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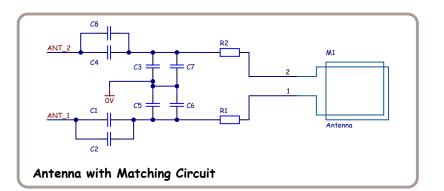




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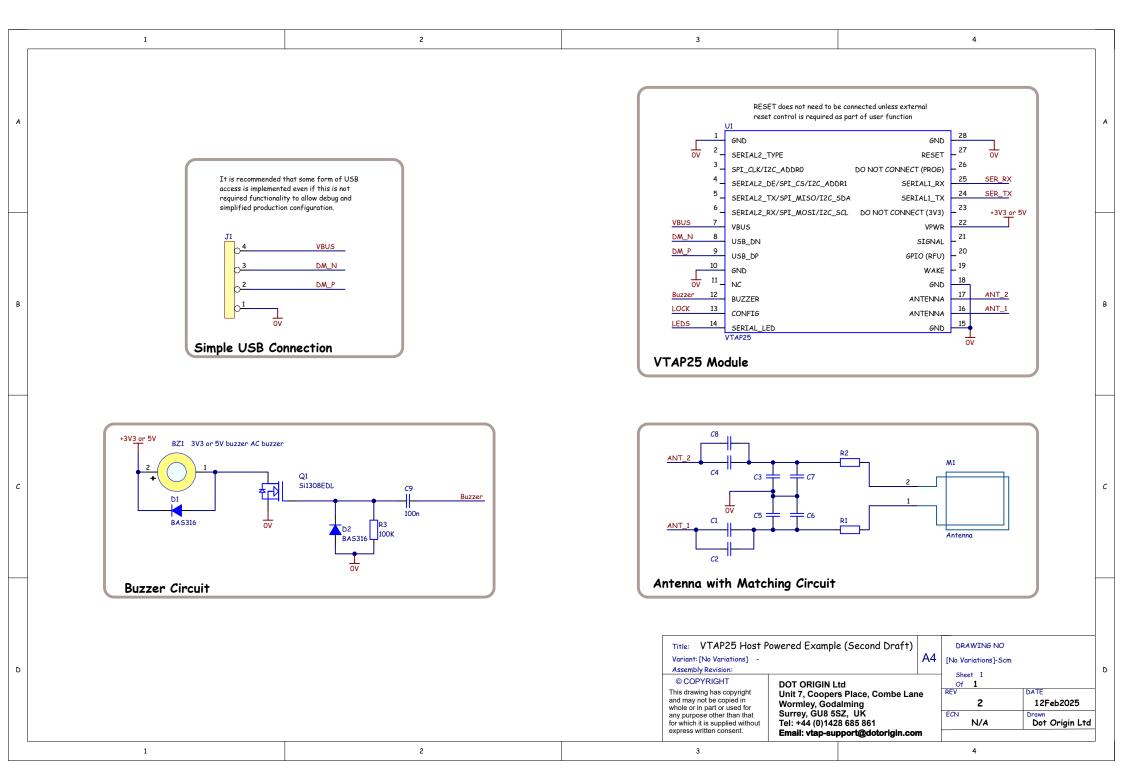
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Title: VTAP25 USB Example (Second Draft) Variant: [No Variations] - Assembly Revision:			A4 DRAWING NO [No Variations]-Scm		D
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3			4		-

## 7.2 VTAP25 host powered example

This example schematic illustrates how to interface a VTAP25 module to a host processor using 3.3V serial UART comms. It includes a buzzer circuit, an antenna with matching circuit and a 4-pin USB connector for backup access to the VTAP25.



## 8 **Recommendations for PCB layout**

#### 8.1 Module dimensions

The module dimensions are 24mm x 29.3mm x 5.9mm (0.95in x 1.15in x 0.23in).

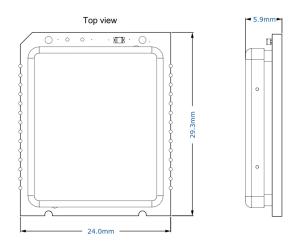


Figure 8-1 VTAP25 reader module dimensions

Please contact **vtap-support@dotorigin.com** for 3D model of the module.

#### 8.1.1 Holes for test pads

To facilitate user tuning, there are six pads inboard on the bottom of the module. The host board must accommodate for these holes for future accessibility. These pads connect to the antenna drive pins on the NFC controller to allow connecting a VNA for tuning purposes and to the receive pins and test-bus pins for future validation. See the VTAP25 footprint for the test pad dimensions.

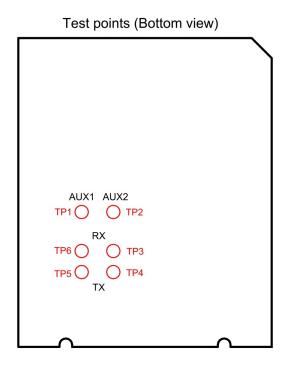


Figure 8-2 VTAP25 reader module test points

## 8.2 Footprint

All dimensions are in mm.

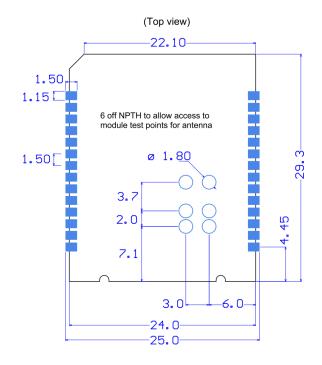


Figure 8-3 VTAP25 reader module footprint

### 8.3 Soldering

Solder the module in a single reflow. Use the lead-free alloy Sn96.5Ag3Cu0.5, also known as the SAC305.

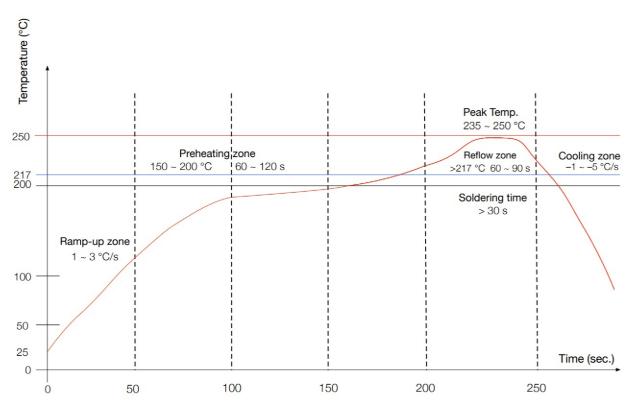


Figure 8-4 VTAP25 reader module solder reflow diagram

The VTAP25 is rated at the moisture sensitivity level (MSL) of 3. Once the module is unpacked from the sealed bags, it must be soldered within 168 hours under the factory conditions  $25 \pm 5^{\circ}$ C and 60 %RH. If not soldered within this time period, the module needs to be baked before soldering.

## 9 Compliance

The VTAP25 module has already been certified for Apple ECP2/Access and Google Smart Tap. Compliance testing is still in progress for compliance with applicable rules for CE, UKCA, FCC, ISED, MIC and Apple VAS. The integrator must usually perform testing of the final product to ensure the compliance is maintained.

Dot Origin can provide support throughout the compliance process. Our engineers have extensive experience of compliance testing and approval processes. Please contact us at **vtap-support@dotorigin.com** at an early stage of your project to discuss the options and recommended steps involved.

PLEASE NOTE THAT SOME OF THIS COMPLIANCE TESTING FOR THE VTAP25 HAS NOT YET BEEN COMPLETED. TESTING IS IN PROGRESS.

# 9.1 CE / UKCA

The VTAP25 will be tested for CE (RED/safety) / UKCA compliance. However, the host product must be tested for all the relevant directives under CE / UKCA.

# 9.2 FCC/ISED

The VTAP25 module will be tested for modular device approval under FCC rules Part 15 and ISED RSS-210, with a reference host board including a 40x40mm NFC antenna.

The final host product, with the VTAP25 module installed, will still require Part 15 Subpart B compliance testing with your NFC antenna. Typically, Dot Origin can obtain a permissive change on the VTAP25 original modular approval. This is faster and less expensive than a new application. In this case, the integrator must ensure that all the guidelines in this document are followed.

Be aware that additional tests can be required on the final integrated system. We recommend integrators refer to further advice from the FCC OET Knowledge Base, such as 996369 D04 Module Integration Guide v02.

# 9.3 Apple VAS and ECP2

The VTAP25 runs the same firmware as VTAP100 and VTAP50 readers, which are already certified for Apple VAS and Apple ECP2 (Access). The VTAP25 is already certified for ECP2/Access and certification is in progress for Apple VAS.

There are some steps required in order to maintain Apple VAS(ECPI) and/or ECP2/Access compliance.

When you request and NFC entitlement and/or permission for an Apple Access deployment we recommend that you inform Apple that a Dot Origin VTAP OEM board or module has been used in your finished product. Apple are aware that our products are available both in finished form and as OEM modules.

- For VAS applications Apple reserves the right to review the final form factor of the reader, to ensure that satisfactory performance and user experience is maintained.
- For ECP2 applications it is essential that the new equipment hosting a VTAP reader board or module is tested and certified against Apple Access specifications. This includes ensuring that the read range meets their minimum distance requirements (40mm) and that the reader is tested against a wide range of different models of iPhone and Apple Watch. Apple may also require on-site functional testing as part of the end-to-end certification of an Apple Access deployment, which is usually conducted by the Credential Manager.

In both cases, our engineering services team is can advise and assist on certification issues, which could include taking a product through formal certification, if required.

## 9.4 Google Smart Tap

The VTAP25 runs the same firmware as VTAP100 and VTAP50 readers, which are already certified for Google Smart Tap. The VTAP25 will also be certified for Google Smart Tap.

The integrator should test the final product with NFC passes in Google Wallet of different Android phones prior to rolling out, to ensure the compliance is maintained.

## 9.5 Recommendations for EMC

To ensure that the final product is compliant with various standards for radiated and conducted emissions, please follow the guidelines in this document relating to USB and antenna track placement and external connections.